CLAIMS

What is claimed is:

1. A processor executing a plurality of instructions, comprising:

an arithmetic logic unit; and

a plurality of registers coupled to the ALU, each register programmable to store a register value;

wherein said processor executes a test and skip instruction that includes a first register reference and a second register reference and causes the processor to compare the register value stored in a register corresponding to the first register reference and a second value associated with the second register reference and to execute or not execute a subsequent instruction that follows the test and skip instruction based on the comparison.

2. The processor of claim 1 wherein the second value comprises a register value stored in the second register reference.

3. The processor of claim 1 wherein the processor is configured to access memory and the second value is stored in the memory.

4. The processor of claim 3 wherein the second register reference contains a value used to compute a pointer to a memory location containing the second value.

5. The processor of claim 4 wherein the pointer is computed by adding the value from the second register reference to a register value from another register.

6. The processor of claim 5 wherein the value held in the another register is post-incremented by a predeterined value following execution of the test and skip instruction.

7. The processor of claim 1 wherein the comparison includes a condition that is specified in the test and skip instruction.

8. The processor of claim 7 wherein any one of a plurality of conditions are specified in the test and skip instruction.

9. The processor of claim 7 wherein the condition is a condition selected the group consisting of equal to, not equal to, less than, and greater than.

10. A method of executing a test and skip instruction, comprising:

examining a bit in the test and skip instruction;

determining an address mode based on said bit;

comparing contents of a first register to contents of a second register if the bit is in a first state; or

comparing the contents of the first register to contents of a non-register location if the bit is in a second state; and

skipping a subsequent instruction based on results of the comparison.

11. The method of claim 10 wherein skipping the subsequent instruction comprises replacing the subsequent instruction with a no operation instruction.

12. The method of claim 10 wherein the non-register location is a location selected from the group consisting of memory and a stack.

13. A system, comprising:

a main processor unit; and

a co-processor coupled to said main processor unit, wherein said co-processor executes a test and skip instruction that includes a first register reference and a second register reference and causes the processor to compare the register value stored in a register corresponding to the first register reference and a second value associated with the second register reference and to execute or not execute a subsequent instruction that follows the test and skip instruction based on the comparison.

14. The system of claim 13 wherein the second value comprises a register value stored in the second register reference.

15. The system of claim 13 wherein the processor is configured to access memory and the second value is stored in the memory.

16. The system of claim 15 wherein the second register reference contains a value used to compute a pointer to a memory location containing the second value.

17. The system of claim 16 wherein the pointer is computed by adding the value from the second register reference to a register value from another register.

18. The system of claim 13 wherein the comparison includes a condition that is specified in the test and skip instruction.

19. The system of claim 18 wherein any one of a plurality of conditions are specified in the test and skip instruction.

20. The system of claim 18 wherein the condition is a condition selected the group consisting of equal to, not equal to, less than, and greater than.

21. The system of claim 13 wherein the system comprises a communication device.

22. A programmable logic device comprising;

control logic; and

a means for executing a test and skip instruction that includes a first register reference identifying a first register having a register value and a second register reference identifying a second register also having a register value, for comparing the register value stored in the first register and a second value associated with the

second register, and for executing or not executing a subsequent instruction that follows the test and skip instruction based on the comparison.

23. The system of claim 22 wherein said second value is stored in a register.

24. The system of claim 22 wherein said second value is stored in memory.

25. The system of claim 22 wherein said second value is stored in a stack.